

60V N-Channel Power Speed FET

• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• Features

- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- AEC-Q101 Qualified

• Application

- BLDC Motor driver
- DC-DC
- Battery protection

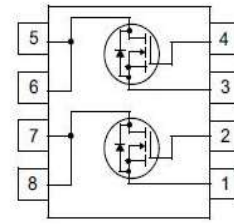
• Ordering Information:

Part NO.	ZMDA68608N
Marking	ZMD68608
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

• Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	52	A
	I_D	$T_C=75^\circ\text{C}$	42	A
	I_D	$T_C=100^\circ\text{C}$	37	A
Pulsed Drain Current ^①	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	208	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	52	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3.0	W
Operating Junction Temperature	T_J		-55 to +175	$^\circ\text{C}$
Storage Temperature	T_{STG}		-55 to +175	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	12	mJ
		$L=0.5\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	21	mJ
ESD Level (HBM)	CLASS 2			

• Product Summary



$V_{DS} = 60\text{V}$
 $R_{DS(ON)} = 7.6\text{m}\Omega$
 $I_D = 52\text{A}$



•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	2.9	°C/W
Thermal resistance, junction-ambient	$R_{thJA\oplus}$		-	50	°C/W
Soldering temperature (total time<10s)	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2	2.6	4	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=60V$	-	-	1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=14A$	-	7.6	9.5	m Ω
Forward Transconductance	g_{FS}	$V_{GS}=5V, I_{SD}=5A$	-	14	-	S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=14A$	-	-	1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	1196	-	pF
Output capacitance	C_{oss}		-	661	-	
Reverse transfer capacitance	C_{rss}		-	47	-	
Gate Resistance	R_g	$f=1MHz$	-	1.2	-	Ω
Total gate charge	Q_g	$V_{DD}=30V, I_D=14A, V_{GS}=10V$	-	19	-	nC
Gate - Source charge	Q_{gs}		-	4.9	-	
Gate - Drain charge	Q_{gd}		-	5.5	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	6	-	ns
Turn-ON Rise time	t_r		-	4	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	11	-	ns
Turn-Off Fall time	t_f		-	7	-	ns
Reverse Recovery Time	t_{rr}	$V_{DD}=20V, dI_S/dt=100A/\mu s, I_S=20A$	-	26	-	ns
Reverse Recovery Charge	Q_{rr}		-	16	-	nC

Fig.1 Gate-Charge Characteristics

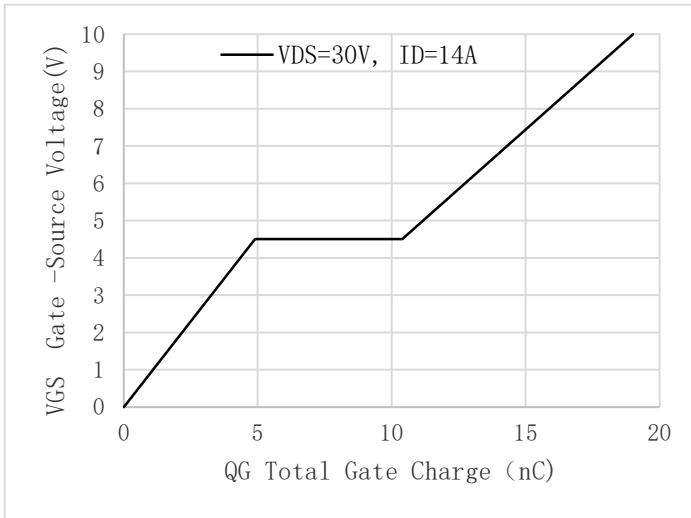


Fig.2 Capacitance Characteristics

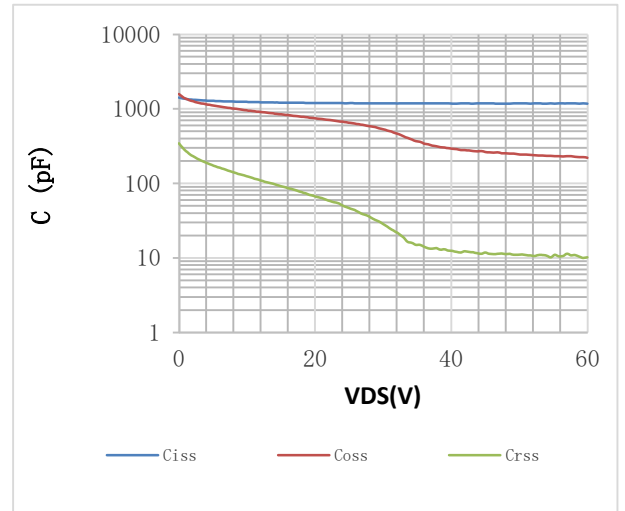


Fig.3 Power Dissipation

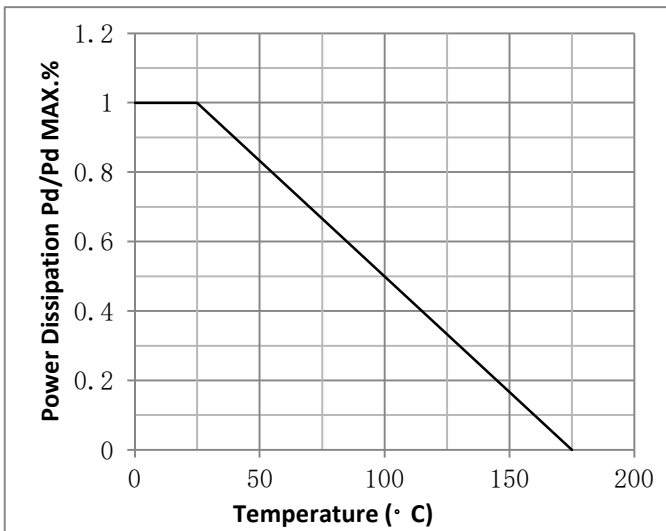


Fig.4 Typical output Characteristics

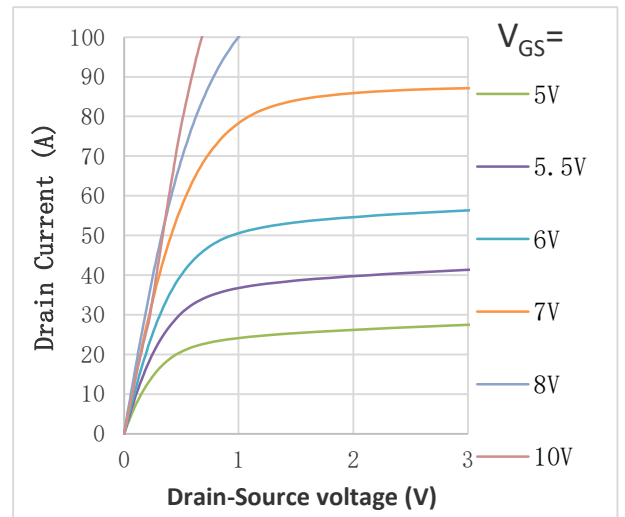


Fig.5 Threshold Voltage V.S Junction Temperature

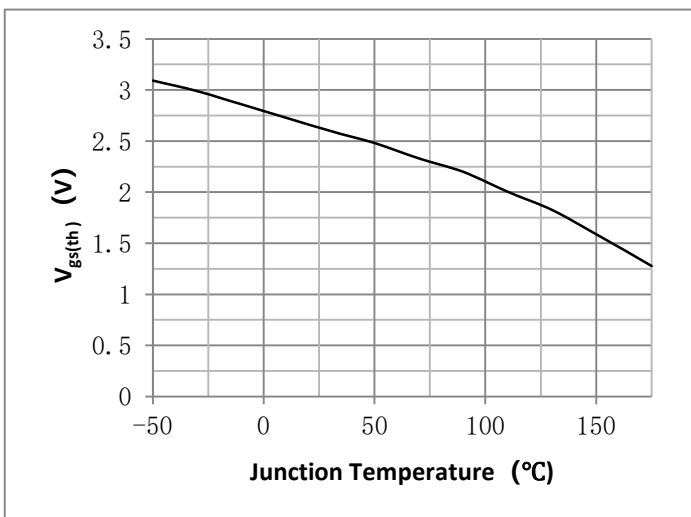


Fig.6 Resistance V.S Drain Current

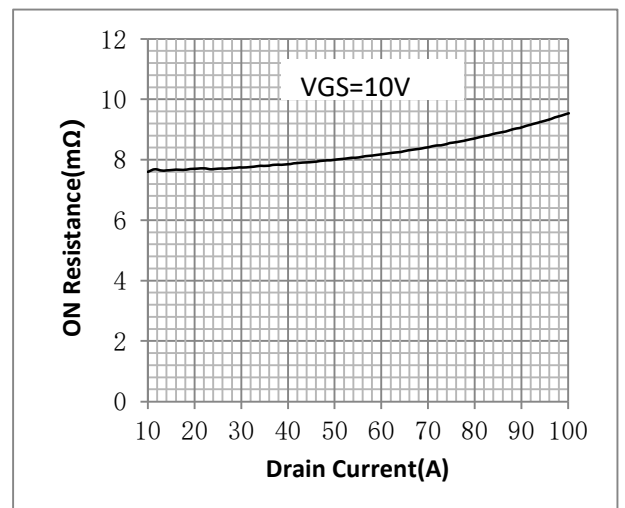


Fig.7 On-Resistance VS Gate Source Voltage

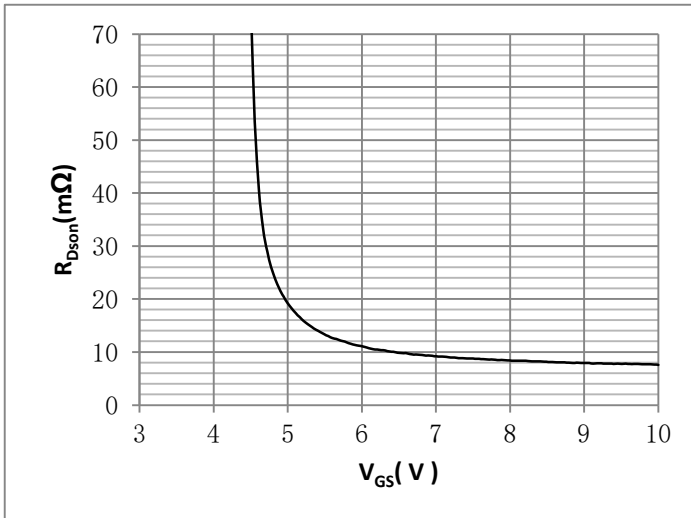


Fig.8 On-Resistance V.S Junction Temperature

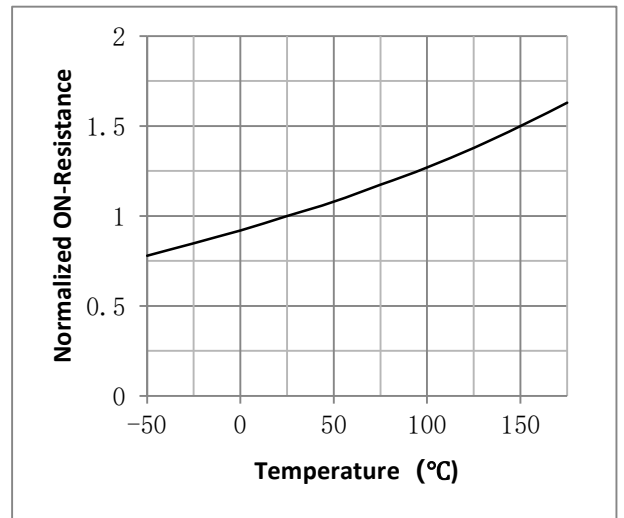


Figure 9. Diode Forward Voltage vs. Current

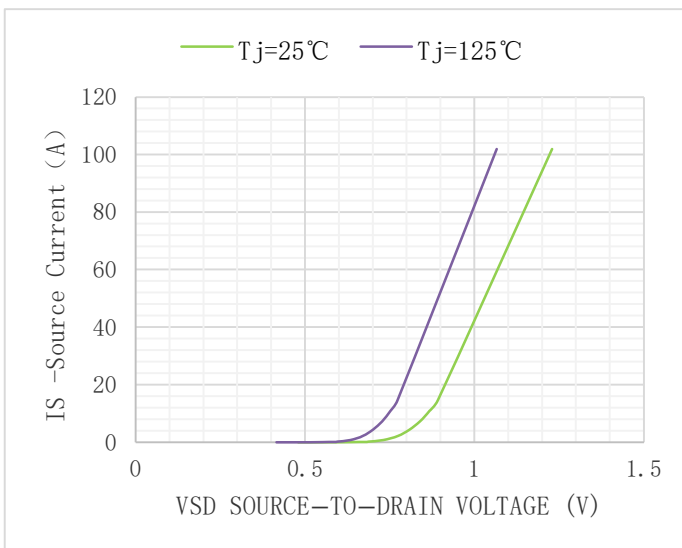


Figure 10. Transfer Characteristics

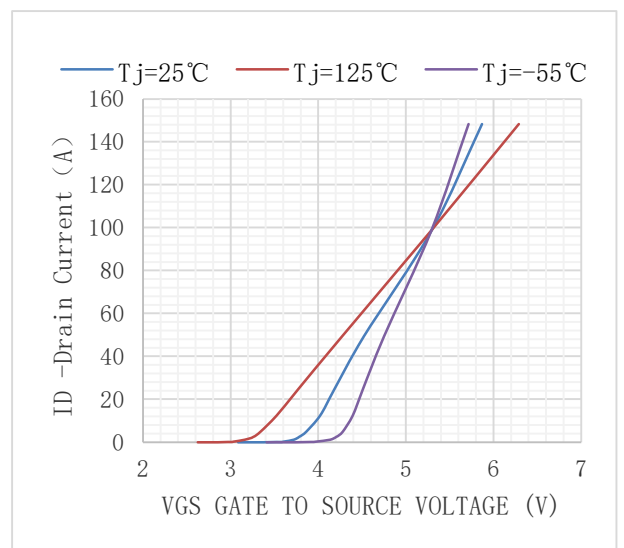


Fig.11 SOA Maximum Safe Operating Area

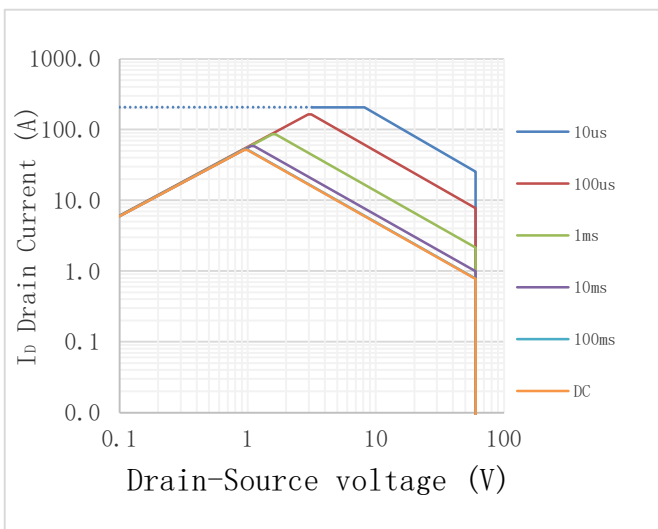
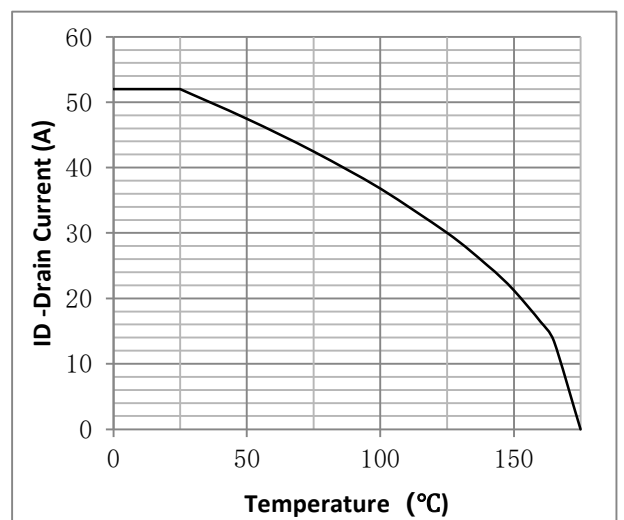
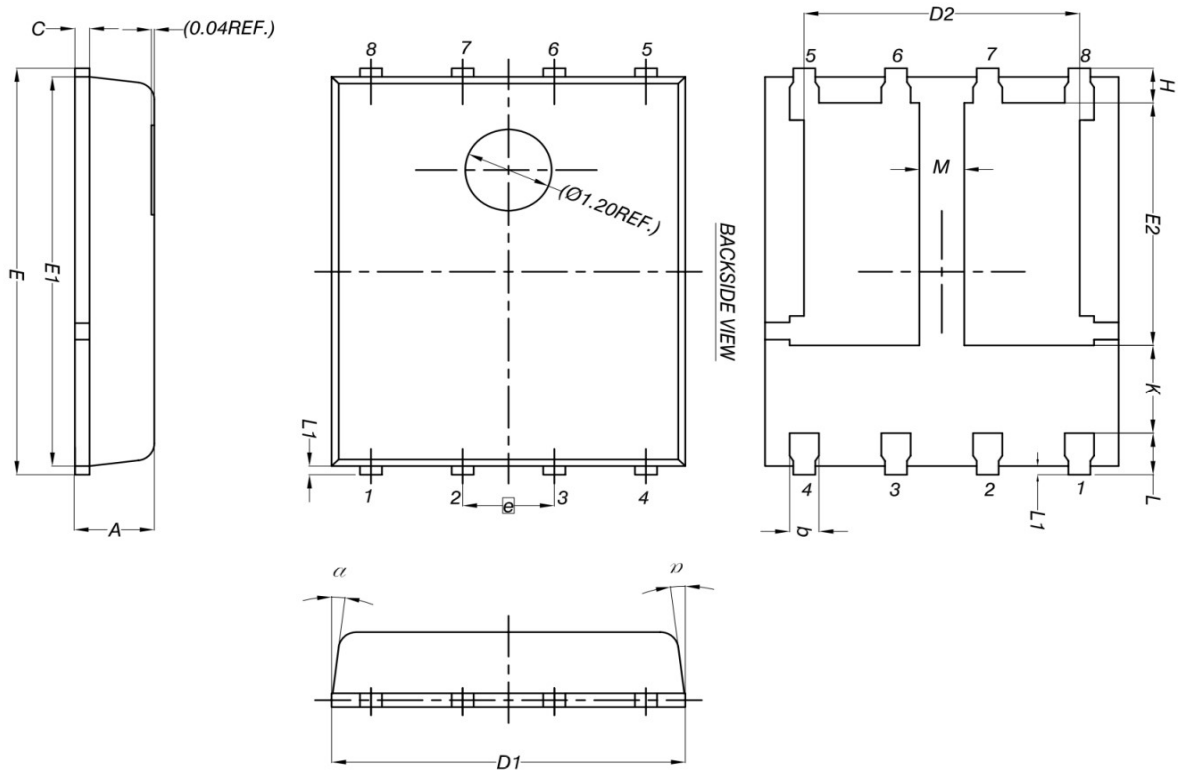


Fig.12 I_D vs. Case Temperature^③

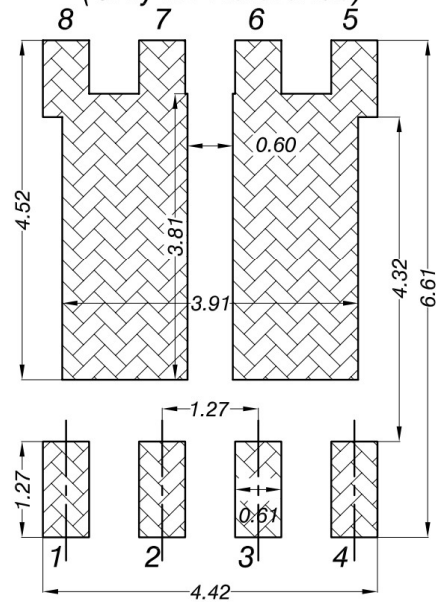


•DFN5*6 Package Outline



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
α	0°	-	12°

Land Pattern
(Only for Reference)



Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature.
 $V_{GS}=10V$.

Disclaimer

- Reproducing and modifying information of the document is prohibited without permission from ZMJ SEMICONDDUCTORS CO.,LTD.
- ZMJ SEMICONDDUCTORS CO.,LTD. reserves the rights to make changes of the content herein the document anytime without notification. Please refer to our website for the latest document.
- ZMJ SEMICONDDUCTORS CO.,LTD. disclaims any and all liability arising out of the application or use of any product including damages incidentally and consequentially occurred.
- ZMJ SEMICONDDUCTORS CO.,LTD. does not assume any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.
- Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. ZMJ SEMICONDDUCTORS CO.,LTD. makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.
- The products shown herein are not designed and authorized for equipments relating to human life and for any applications concerning life-saving or life-sustaining, such as medical instruments, aerospace machinery et cetera. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify ZMJ SEMICONDDUCTORS CO.,LTD. for any damages resulting from such improper use or sale.
- Since ZMJ uses lot number as the tracking base, please provide the lot number for tracking when complaining.

Revision History

Version	Date	Change
A	2024.12.19	New